ECUcore-E660

Hardware Manual

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详情请通过sales@hkaco.com联系我们

北京：010-5781 5068
上海：021-6728 3703
广州：020-3874 3032
西安：029-8187 3816

System House for Distributed Automation

Status / Changes

Status: released

Date/ Version	Section	Change	Editor
L-1562e_01		initial version	B. Rudert

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1st Edition July 2014

Index of figures and tables

1 Introduction

This manual describes the function and technical data for the ECUcore-E660, but not for the microprocessor Intel Atom E660 or any other supplemental products. Please refer to the corresponding manuals and documentation for any other products you may use.

Low-active signals are denoted by a „/“ in front of the signal name (i.e. “/RD”). The representation “0” indicates a logical-zero or low-level signal. A “1” is the synonym for a logical one or high-level signal.

2 Ordering Information and Support

Order Number	Version
4001027	ECUcore-E660
4002016	Development Kit ECUcore-E660

The ECUcore-E660 features:

- High-performance CPU kernel (Intel Atom E660 1.3 GHz CPU at 1.0 GHz, 512KiB L2-Cache)
- 1 GByte SDRAM Memory, 4GByte FLASH Memory
- 1 MiB dedicated Video RAM
- LVDS LCD Controller supports up to 1280x768 pixel resolution with 24-bit color depth
- SDVO LCD Interface supports up to 1280x1024 pixel @ 85 Hz resolution with 24-bit color depth
- 6 USB Host interfaces
- 1 USB Device interfaces
- Possibility for connecting HMI devices such as USB Keyboard, USB Mouse and DVI Graphic Cards
- 2x 10/100/1000 Mbps Ethernet LAN interface
- 2x CAN 2.0B interface, usable as CANopen Manager
- 4x asynchronous serial ports (UART)
- 14 General purpose digital in/ouputs
- Externally usable SPI and I2C
- SMBus and LPC Bus
- On-board peripherals: RTC, temperature sensors, watchdog, SDC , Single power supply 5V (all other voltages are derived on-board)
- ESD Handling Instructions (printed version)

Making available a complete single board computer subassembly as an insert-ready core module with small dimensions, reduces effort and costs significantly for the development of user-specific controls. The ECUcore-E660 is also very well suitable as basic component for custom specific HMI devices as well as an intelligent network node for decentralized processing of process signals.

The default I/O configuration can be adapted for specific application requirements by using the Driver Development Kit (SO-1117). Saving the user application in

the on-board Flash-Disk of the module allows an automatic restart in case of power breakdown.

Das ECUcore-E660 is based on Embedded Linux as operating system. This allows for simultaneous execution of several user-specific programs.

The Embedded Linux applied to the ECUcore-E660 is licensed under GNU General Public License, version 2. Appendix A contains the license text. All sources of LinuxBSP are included in the VMware-Image of the Linux development system (SO-1116). If you require the LinuxBSP sources independently from the VMware-Image of the Linux development system, please contact our support:

3 Properties of the ECUcore-E660

3.1 Overview

The ECUcore-E660 is another innovative product that extends the SYS TEC electronic GmbH product range within the field of control applications. In the form of an insert-ready core module (“Core”), it provides to the user a complete single board computer subassembly that is programmable under Linux and has available an integrated Target Visualization. Due to CAN, USB and Ethernet interfaces, the ECUcore-E660 is best suitable to realize custom specific HMI (**H**uman **M**achine **I**nterface) applications.

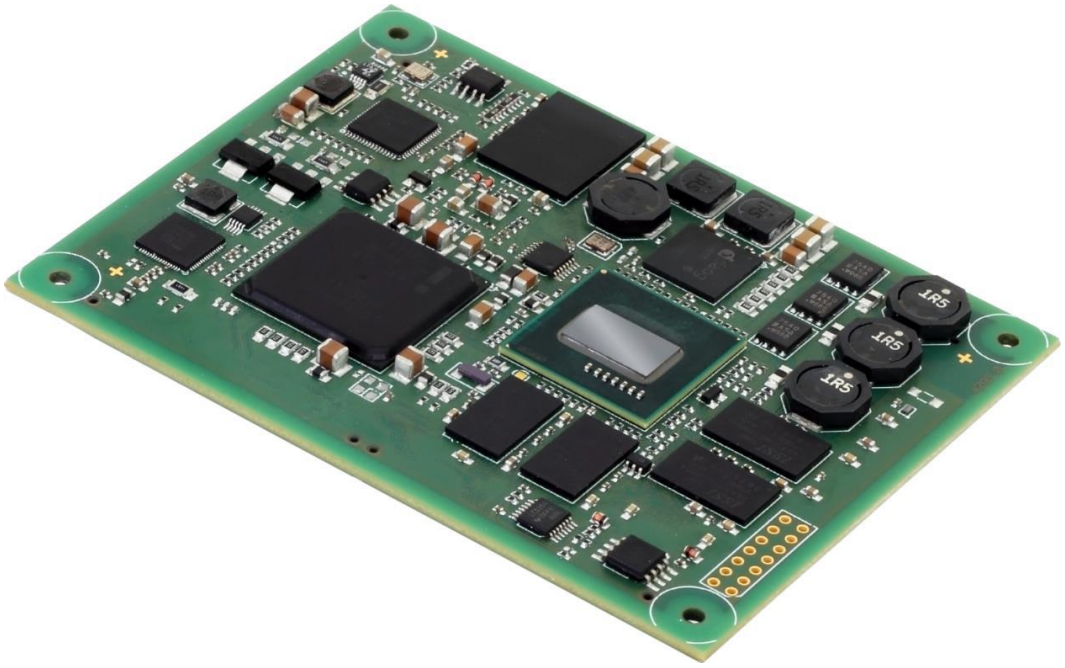

Figure 1: ECUcore-E660

The dimensions of the board are 105 mm x 80 mm and it includes four board connectors which makes it multifunctional in embedded systems.

The ECUcore-E660 features an Intel Atom E660T microprocessor. It is a highly-integrated 32-bit microprocessor based on the Intel x86 “Tunnel Creek” architecture.

The interconnection to a customer board is possible through a pair of low-density (0,8mm pitch) connectors with 320 pins in total.

The ECUcore-E660 includes the following features:

- Internal features of the Intel Atom E660:
    - Internal 1,3 GHz CPU-clock
    - On die, 32 kB 4-way L1 Instruction Cache and 24 kB 6-way L1 Data Cache
    - On die, 512 kB, 8-way L2 cache
    - 32-bit physical address, 48-bit linear address size support
    - Image processing unit (IPU)
    - Support for IA 32-bit architecture
    - Supports Intel® Virtualization Technology
    - (Intel® VT-x)
    - Supports Intel® Hyper-Threading Technology — two threads
    - Advanced power management features including Enhanced Intel SpeedStep® Technology
    - Deep Power Down Technology (C6)
    - Intel® Streaming SIMD Extension 2 and 3 (Intel® SSE2 and Intel® SSE3) and Supplemental Streaming SIMD Extensions 3 (SSSE3) support
    - Single-channel DDR2 memory controller
    - 32-bit data bus
    - Supports DDR2 800 MT/s data rates
    - Integrated 2D/3D graphic engine
    - LVDS Interface, maximum resolution 1280x768@60Hz, 18 or 24bpp
    - Serial DVO Display Interface, maximum resolution 1280x1024@ 85Hz.
    - PCI Express 1.0a, 4 independent x1 lanes
    - LPC Interface, for attaching ISA bus based devices

  - SMBus Host Controller for I²C bus based devices
  - Intel HD Audio Controller
  - 14 GPIO pins
  - 1 SPI interface (SPI) for BIOS boot
  - Power Management: Suspend-to-RAM, Suspend-to-Disk and ACPI support
  - Watchdog (WDT) (1µs to 10min)
  - Real Time Clock (RTC)
  - 3,6 Watt TDP

- Memory configuration:

  - up to 4GiByte eMMC
  - up to 1GiByte DDR2 RAM

- Communication features:

  - 2 10/100/1000 Ethernet interfaces
  - LPC interface
  - 2 SATA II host interfaces
  - 4 UARTs
  - 1 CAN as LVTTL
  - 1 USB device high speed
  - 6 USB host high speed
  - 1 SMBus interface
  - 1 µSDHC up to 32GiB
  - 1 additional USART via System Diagnose Controller (SDC)
  - 1 additional I²C via System Diagnose Controller (SDC)
  - 1 additional CAN via System Diagnose Controller (SDC)

- Other board-level features:

  - 2 Ethernet PHY
  - SROM for BIOS Confiuration
  - ARM9 System Diagnose Controller with ADC (connected by SMBus)
  - LVDS controller

- Temperature sensor
- 5V operating voltage
  on-board generated voltage for CPU
- Industrial temperature range (-40°C to +85°C)
- RoHS compliant
- ADC via SDC

3.2 Block Diagram

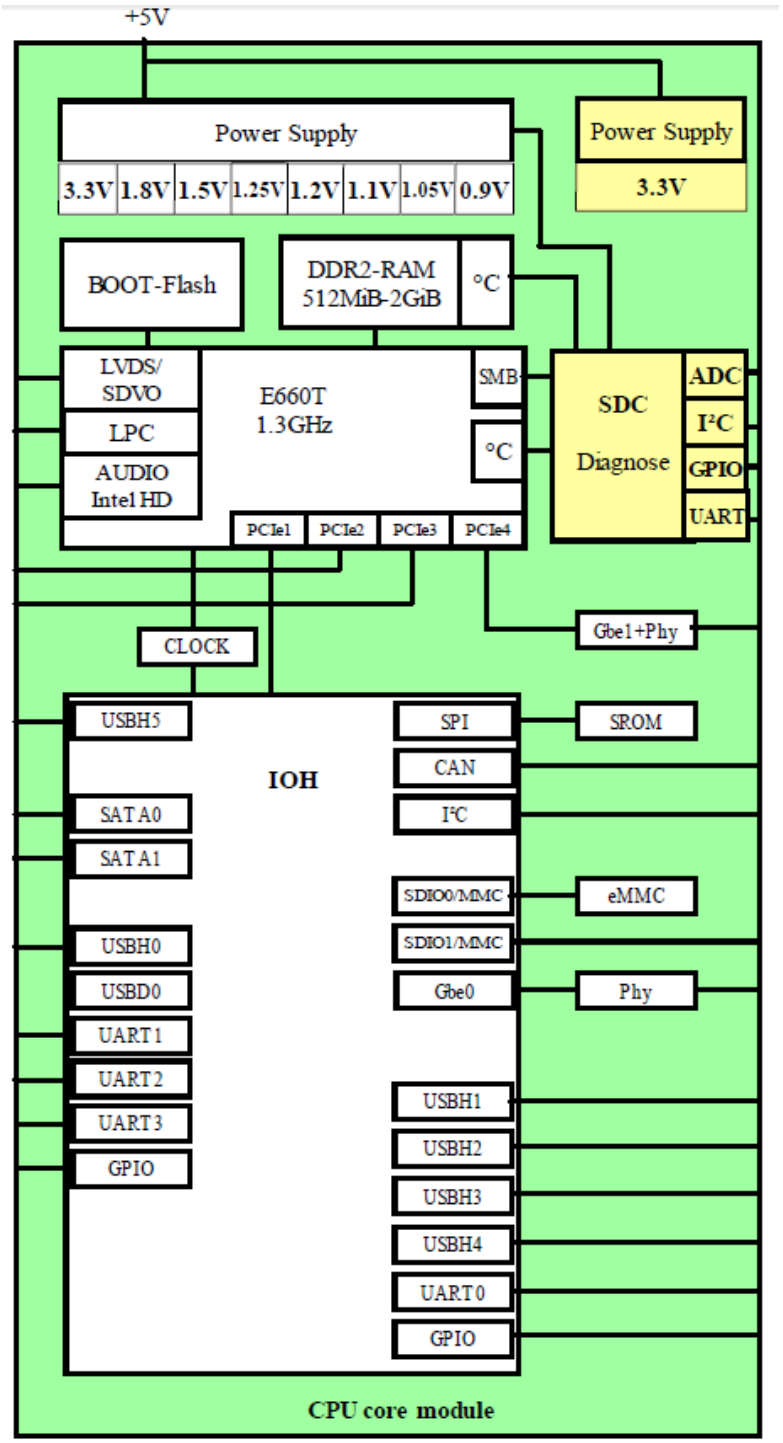

Figure 2: Block Diagram ECUcore-E660

4 Component Descriptions

The functions of the on-board components are explained in the following sections.

4.1 Connectors

The ECUcore-E660 has two board connectors. Each of the SMT socket strips consists of 100 contacts divided into double rows. In total the module has 200 contacts. For better EMC-properties, 20% of the pins are GND.
A third connector at the front side is for connecting debug interfaces of the CPU and the signal /DIS_NAND.

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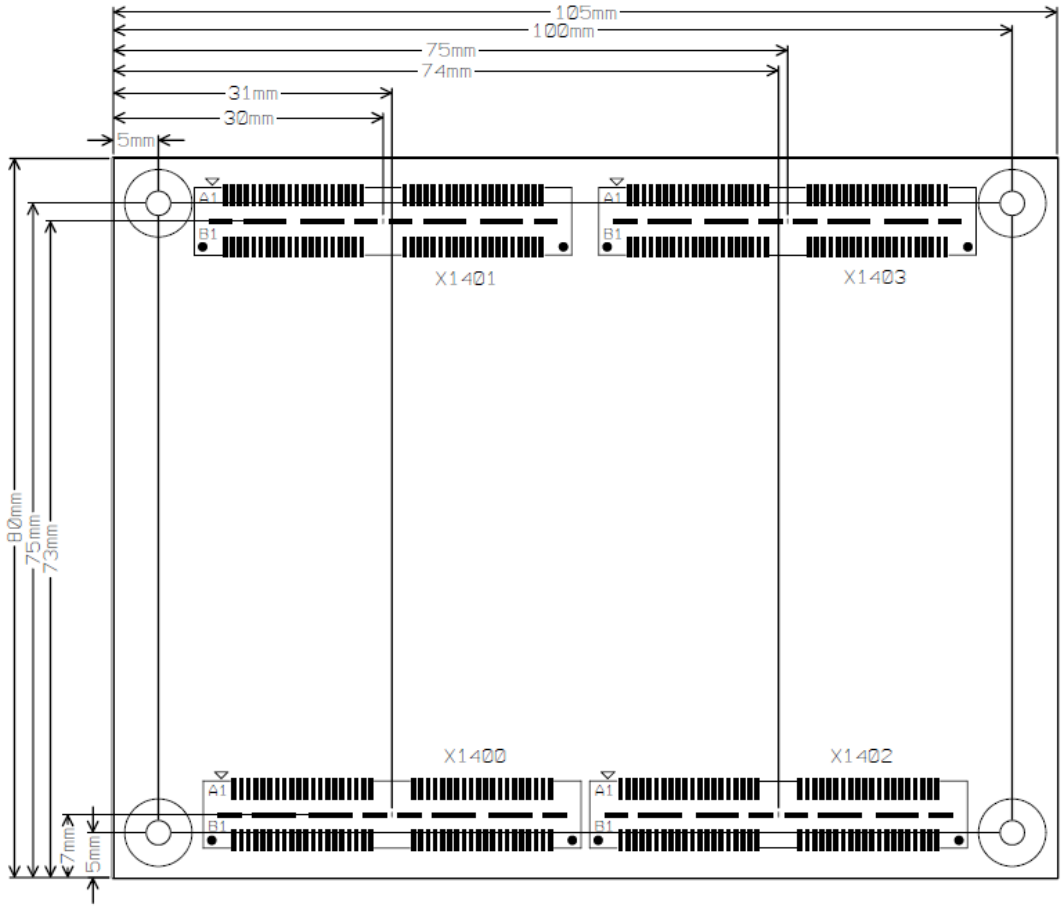

Figure 3: Pinout (Top View)

The picture shows the module from top view which means you look from the top through the module. The connectors are placed accordingly to the ones on the customer board.

The board connectors are equipped with the common and durable 0,8mm pitch. The type of mezzanine socket stripes used on the ECUcore-E660 is “Q Strip”®-series provided by "SAMTEC" with a height of 3,25mm.

Connectors:
ECUcore-E660:

4 x Samtec QSE-040-01-F-D-A-K-TR (2x40pol. socket)

Customer board:

4 x Samtec QTE-040-01-F-D-A-K (2x40pol. header)

Table 1, Table 2, Table 3 and Table 4 define the pin out.

Signal	Pin	Pin	Signal
ETH0_MDI_3-	A01	B01	/LPC_FRAME_B
ETH0_MDI_3+	A02	B02	LPC_AD0
GND	A03	B03	LPC_AD1
ETH0_MDI_2-	A04	B04	LPC_AD2
ETH0_MDI_2+	A05	B05	LPC_AD3
ETH0_LED1	A06	B06	LPC_CLKOUT0
ETH0_MDI_1-	A07	B07	LPC_CLKOUT1
ETH0_MDI_1+	A08	B08	LPC_CLKOUT2
ETH0_LED2	A09	B09	LPC_SERIRQ
ETH0_MDI_0-	A10	B10	SMB_CLK_EXT
ETH0_MDI_0+	A11	B11	SMB_DATA_EXT
GND	A12	B12	/SMB_ALERT_EXT
SATA0_TX_+	A13	B13	SATA1_TX_+
SATA0_TX_-	A14	B14	SATA1_TX_-
SATA0_RX_+	A15	B15	SATA1_RX_+
SATA0_RX_-	A16	B16	SATA1_RX_-
SATA0_LED	A17	B17	SATA1_LED
HAD_SYNC	A18	B18	HDA_SDI1
/HDA_RST	A19	B19	HAD_SDI0
HDA_CLK	A20	B20	/HAD_DOCKEN
GND	GND1		
HDA_SDO	A21	B21	/HAD_DOCKRST
USB_H4_POW_EN	A22	B22	USB_H5_POW_EN
/USB_H4_OVC	A23	B23	/USB_H5_OVC
USB_H4_-	A24	B24	USB_H5_-
USB_H4_+	A25	B25	USB_H5_+
USB0H2_POW_EN	A26	B26	USB_H3_POW_EN
/USB_H2_OVC	A27	B27	/USB_H3_OVC
USB_H2_-	A28	B28	USB_H3_-
USB_H2_+	A29	B29	USB_H3_+
USB_H0_POW_EN	A30	B30	USB_H1_POW_EN
/USB_H0_OVC	A31	B31	/USB_H1_OVC
USB_H0_-	A32	B32	USB_H1_-
USB_H0_+	A33	B33	USB_H1_+
USB_D_-	A34	B34	I2C_CLK
USB_D_+	A35	B35	I2C_DATA
/COLD_RESET	A36	B36	PWROK
ATOM_WD	A37	B37	SPEAKER
/CPU_THERMTRIP	A38	B38	/CPU_OVT
/WARM_RESET	A39	B39	/CPU_RESET
VBAT_RTC	A40	B40	/CPU_PROCHOT
GND	GND2		

Table 1: Pin out connector X1400

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Signal	Pin	Pin	Signal
ETH1_MDI_3-	A01	B01	1V9_LAN
ETH1_MDI_3+	A02	B02	1V9_LAN
ETH1_LED0	A03	B03	CAN_RX
ETH1_MDI_2-	A04	B04	CAN_TX
ETH1_MDI_2+	A05	B05	SROM_CLK
ETH1_LED1	A06	B06	/SROM_CS
ETH1_MDI_1-	A07	B07	SROM_DIN
ETH1_MDI_1+	A08	B08	SROM_DOUT
ETH1_LED2	A09	B09	NC_SI_CLK_IN
ETH1_MDI_0-	A10	B10	NC_SI_TX_EN
ETH1_MDI_0+	A11	B11	NC_SI_CRS_DV
SDIO1_PWR_EN	A12	B12	NC_SI_RXD0
SDIO1_LED	A13	B13	NC_SI_TXD0
SDIO1_D0	A14	B14	NC_SI_RXD1
SDIO1_D1	A15	B15	NC_SI_TXD1
SDIO1_D2	A16	B16	SDIO1_D4
SDIO1_D3	A17	B17	SDIO1_D5
SDIO1_CLK	A18	B18	SDIO1_D6
SDIO1_CMD	A19	B19	SDIO1_D7
SDIO1_CARD_WP	A20	B20	/SDIO1_CARD_DET
GND	GND1		
SPI2_CS	A21	B21	SPI2_CLK
SDC_CLK	A22	B22	SPI2_MISO
SDC_GPIO_1	A23	B23	SPI2_MOSI
SDC_GPIO_2	A24	B24	SDC_NJTRST
SDC_GPIO_3	A25	B25	SDC_TDO/TRACESWO
SDC_GPIO_4	A26	B26	SDC_TDI
SDC_GPIO_5	A27	B27	SDC_TMS/SWDIO
SDC_GPIO_6	A28	B28	SDC_TCK/SWCLK
SDC_GPIO_7	A29	B29	SDC_GPIO_15
SDC_GPIO_8	A30	B30	SDC_GPIO_16
SDC_GPIO_9	A31	B31	SDC_GPIO_17
SDC_GPIO_10	A32	B32	SDC_GPIO_18
SDC_GPIO_11	A33	B33	SDC_GPIO_19
SDC_GPIO_12	A34	B34	SDC_GPIO_20
SDC_GPIO_13	A35	B35	SDC_GPIO_21
SDC_GPIO_14	A36	B36	SDC_GPIO_22
SDC_USART1_RX	A37	B37	SDC_GPIO_23
SDC_USART1_TX	A38	B38	SDC_GPIO_24
SDC_CANRX	A39	B39	SDC_GPIO_25
SDC_CANTX	A40	B40	SDC_GPIO_26
GND	GND2		

Table 2: Pin out connector X1401

Signal	Pin	Pin	Signal
PCIE_TX3_+	A01	B01	PCIE_RX3_+
PCIE_TX3_-	A02	B02	PCIE_RX3_-
PCIE_TX2_+	A03	B03	PCIE_RX2_+
PCIE_TX2_-	A04	B04	PCIE_RX2_-
USER_PCIE_CLK_+	A05	B05	SDIO0_PWR_EN
USER_PCIE_CLK_-	A06	B06	SDIO0_LED
SDIO0_CARD_WP	A07	B07	/SDIO0_CARD_DET
SDIO0_D0	A08	B08	SDIO_D4
SDIO0_D1	A09	B09	SDIO_D5
SDIO0_D2	A10	B10	SDIO_D6
SDIO0_D3	A11	B11	SDIO_D7
SDIO0_CLK	A12	B12	SDIO_CMD
LVDS_DATA0_+	A13	B13	SDVO_RED_+
LVDS_DATA0_-	A14	B14	SDVO_RED_-
LVDS_DATA1_+	A15	B15	SDVO_GREEN_+
LVDS_DATA1_-	A16	B16	SDVO_GREEN_-
LVDS_DATA2_+	A17	B17	SDVO_BLUE_+
LVDS_DATA2_-	A18	B18	SDVO_BLUE_-
LVDS_DATA3_+	A19	B19	SDVO_INT_+
LVDS_DATA3_-	A20	B20	SDVO_INT_-
GND	GND1		
LVDS_CLK+	A21	B21	SDVO_CLK_+
LVDS_CLK-	A22	B22	SDVO_CLK_-
SPI_MISO	A23	B23	SDVO_TVCLKIN_+
SPI_CLK	A24	B24	SDVO_TVCLKIN_-
SPI_MOSI	A25	B25	SDVO_STALL_+
/SPI_CS	A26	B26	SDVO_STALL_-
UART0_TX	A27	B27	SDVO_CTRLCLK
UART0_RX	A28	B28	SDVO_CTRLDATA
UART1_TX	A29	B29	UART0_CTS
UART1_RX	A30	B30	UART0_DCD
UART2_TX	A31	B31	UART0_DSR
UART2_RX	A32	B32	UART0_DTR
UART3_TX	A33	B33	UART0_RI
UART3_RX	A34	B34	UART0_RTS
VCC_5V0	A35	B35	VCC_5V0
VCC_5V0	A36	B36	VCC_5V0
VCC_5V0	A37	B37	VCC_5V0
VCC_5V0	A38	B38	VCC_5V0
VCC_5V0	A39	B39	VCC_5V0
VCC_5V0	A40	B40	VCC_5V0
GND	GND2		

Table 3: Pin out connector X1402

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Signal	Pin	Pin	Signal
SDC_BOOT0	A01	B01	SDC_GPIO_27
SDC_BOOT1	A02	B02	SDC_GPIO_28
Unused	A03	B03	/CPU_WAKE
Unused	A04	B04	/MR
IO_PWROK	A05	B05	ADC_IN_2
Unused	A06	B06	ADC_IN3
H_GPIO0	A07	B07	A_GPIO_0
H_GPIO1	A08	B08	A_GPIO_1
H_GPIO2	A09	B09	A_GPIO_2
H_GPIO3	A10	B10	A_GPIO_3
H_GPIO4	A11	B11	A_GPIO_4
H_GPIO5	A12	B12	A_GPIO_SUS_0
H_GPIO6	A13	B13	A_GPIO_SUS_1
H_GPIO7	A14	B14	A_GPIO_SUS_2
H_GPIO8	A15	B15	A_GPIO_SUS_3
H_GPIO9	A16	B16	A_GPIO_SUS_4
H_GPIO10	A17	B17	A_GPIO_SUS_5
H_GPIO11	A18	B18	A_GPIO_SUS_6
Unused	A19	B19	A_GPIO_SUS_7
Unused	A20	B20	A_GPIO_SUS_8
GND	GND1		
HUB_TCK	A21	B21	ETH_TCK
HUB_TMS	A22	B22	ETH_TMS
HUB_TDI	A23	B23	ETH_TDI
HUB_TDO	A24	B24	ETH_TDO/WAKE
/HUB_TRST	A25	B25	IO_TCK
HUBRTCK	A26	B26	IO_TMS
CPU_TCK	A27	B27	IO_TDI
CPU_TMS	A28	B28	IO_TDO
CPU_TDI	A29	B29	/IO_TRST
CPU_TDO	A30	B30	NC_TCK
/CPU_TRST	A31	B31	NC_TMS
DS_TCK	A32	B32	NC_TDI
DS_TMS	A33	B33	NC_TDO
DS_TDI	A34	B34	Unused
DS_TDO	A35	B35	Unused
VCC_5V0	A36	B36	VCC_5V0
VCC_5V0	A37	B37	VCC_5V0
VCC_5V0	A38	B38	VCC_5V0
VCC_5V0	A39	B39	VCC_5V0
VCC_5V0	A40	B40	VCC_5V0
GND	GND2		

Table 4: Pin out connector X1403

Pin function:

Name	Function
SDC_BOOTx	for selecting boot mode of System Diagnostic Controller
/MR	manual reset input of module
/CPU_RESET	reset input signal for the CPU
SATAx_TX+, SATAx_TX-, SATAx_RX+, SATAx_RX-, SATAx_LED	SATA 0, 1 with Busy-LED
ATOM_WD	watchdog input for whole core module
LPC_xyz	LPC Interface Signals . (further information at Intel® AtomE6xx Series Datasheet)
HDA_xyz	Connectors for Intel® HD Audio interfaces. (further information at Intel® AtomE6xx Series Datasheet)
USB_Hx_POW_EN	Power enable signal for USB Host (0 to 5) interfaces
/USB_Hx_ÖVC	USB Host (0 to 5) overcurrent indication
USB_Hx_+, USB_Hx_-	USB Host (0 to 5) differential bus signals
PCIE_TXx_+, PCIE_TXx_-, PCIE_RXx_+, PCIE_RXx_-	PCIExpress (lane 2 and 3) differential bus signals
USER_PCIE_CLK_+, USER_PCIE_CLK_-	PCIExpress differential clock signal
SMB_CLK_EXT, SMB_DATA_EXT, /SMB_ALERT_EXT	SMBus Interface Signals
UARTx_TX, UARTx_RX,	UART 0,1,2,3
UART0_CTS, UART0_DCD, UART0_DSR, UART0_DTR, UART0_RI, UART0_RTS	UART 0 handshake signals
SDIOx_CMD, SDIOx_CLK, SDIOx_DATA,	SD-Card 0,1 interface pins
/SDIOx_CARD_DET	SD-Card 0,1 card detect pins
SDIOx_LED	SD-Card 0,1 busy led
SDIOx_CARD_WP	SD-Card 0,1 Wake-up card signal
I2C2_DAT, I2C2_CLK	two wire interface
SDVO_xyz	Serial Digital Video Output . (further information at Intel® Atom E6xx Series Datasheet)
SDC_GPIO_x	GPIOs provided by STM32 System Diagnostic Controller (SDC)
A_GPIO_SUS_x, A_GPIO_x	GPIOs provided by Intel Atom E660T processor
H_GPIO_x	GPIOs provided by Intel EG20T hub IC
NC_SI_xyz	Pins for Network Controller Sideband Interface
SDC_USART1_RX, SDC_USART1_TX	UART of SDC
SPIx_CLK, SPIx_MISO, SPIx_MOSI	SPI 1,2 clock and data signals
SROM_DIN, SROM_DOUT, /SROM_CS, SROM_CLK	SROM Interface of EG20T Hub
VBAT	backup battery input (3,3V) for RTC
ETHx_TX-, TX+, RX-, RX+; LEDx	Ethernet-interfaces with LEDs
SPEAKER	PWM driven beeper output
HUB_TCK,HUB_TMS, HUB_TDI, HUB_TDO, /HUB_TRST, HUB_RTCK	JTAG interface for EG20T hub
ETH_TCK, ETH_TMS, ETH_TDI, ETH_TDO	JTAG interface for Intel Ethernet Controller
IO_TCK, IO_TMS, IO_TDI, IO_TDO, /IO_TRST	IO JTAG of Atom E660T
NC_TCK, NC_TMS, NC_TDI, NC_TDO	JTAG for internal network controller of Atom E660T
CPU_TCK, CPU_TMS, CPU_TDI, CPU_TDO, CPU_TRST_B	JTAG of CPU Atom E660T
SDC_TCK, SDC_TMS, SDC_TDI, SDC_TDO, SDC_NJTRST	JTAG for system diagnostic controller (SDC)
DS_TCK, DS_TMS, DS_TDI, DS_TDO	JTAG of Reset -/ Power Controller
+3V3	3,3V-supply (about 820mA)

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GND	Signal ground

Table 5: Signal description connector X1400/X1401/X1402/X1403

4.2 Power Supply

The ECUcore-E660 must be supplied with an input voltage of +5VDC.

The 5V directly supplies only the DA6011 power supply IC, which supplies all necessary voltages for the core module.

Reset Controller

The Reset Controlling Unit consists of functionality of power supply unit and the System Diagnostic Controller (SDC). The SDC is responsible to handle start-up, wake-up and reset scenarios.

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4.3 SDRAM

The Intel® Atom™ Processor E6xx Series contains an integrated 32-bit single-channel memory controller that supports DDR2 memory in soldered down DRAM configurations only. The memory controller supports data rates of 800 MT/s. There is no support for ECC in the memory controller.

The RAM density is 8x1Gb.

By default, a RAM with 5ns cycle time for 200MHz bus frequency is mounted.

Memory Clock	DRAM Clock	DRAM Data Rate	DRAM Type	Peak Bandwith
200 MHz	400 MHz	800MT/s	DDR2	3,2Gb/s

4.4 NAND-Flash

The board is equipped with NAND-Flash.
The Flash (default: 1x NAND16GAH) is connected on standard SD Host controller of EG20T Hub by using eMMC standard. It works with up to 52 Mbyte/s data transfer rate. The density is up to 4GiByte .

4.5 Ethernet Controller

The E660 supports two 10/100/1000MBit/s Ethernet channels.
One on-board PHY chip KSZ9021GNI/KSZ9031MNX allows a 10/100/1000 MBit/s physical interface. The PHY is connected with the MII interface of the EG20T Hub.
The second Ethernet PHY (Intel 82574) is an all-in-one (MAY+PHY) solution connected by one PCIExpress lane directly to Atom E660T processor.

Board connector signals are:

Signal	Description
ETHx_MDI_3+	BI_DD+ (only at 1000BaseT)

ETHx_MDI_3-	BI_DD- (only at 1000BaseT)
ETHx_MDI_2+	BI_DC+ (only at 1000BaseT)
ETHx_MDI_2-	BI_DC- (only at 1000BaseT)
ETHx_MDI_1+	BI_DA+ (MDI-X) / BI_DB+ (MDI) → TX+
ETHx_MDI_1-	BI_DA- (MDI-X) / BI_DB- (MDI) → TX-
ETHx_MDI_0+	BI_DA+ (MDI) / BI_DB+ (MDI-X) → RX+
ETHx_MDI_0-	BI_DA- (MDI) / BI_DB- (MDI-X) → RX-
ETH1_LED0	output of PHY-LED0 (only on ETH1)
ETHx_LED1	output of PHY-LED1
ETHx_LED2	output of PHY-LED2

Table 6: Ethernet signals

There are no push-/pull-resistors on MDI Signals on-board. So you probably need to add them additional to the transformer and connector as external components for communication.

SYS TEC electronic has acquired a pool of MAC addresses. The MAC address for the first Ethernet interface Eth0 is barcode-labelled and attached on the ECUcore-E660.

4.6 I2C Module

The ECUcore-E660 features one I2C interface. This is a 2-wire serial bus used for communication with I2C devices. The bus is brought out via the board connector.

4.7 Real Time Clock

The Atom E660T processor is equipped with a Real time clock to manage real-time applications.
The Real Time Clock (RTC) module provides a battery backed-up date and time keeping device. Three interrupt features are available: time of day alarm with once a second to once a month range, periodic

rates of 122 μs to 500 ms, and end of update cycle notification. Seconds, minutes, hours, days, day of week, month, and year are counted.

The hour is represented in twelve or twenty-four hour format, and data can be represented in BCD or binary format. The design is meant to be functionally compatible with the Motorola MS146818B. The time keeping comes from an external 32.768 kHz oscillating source, which is divided to achieve an update every second.

4.8 SMBus

The System Management Bus (abbreviated to SMBus or SMB) is a single-ended simple two-wire bus for the purpose of lightweight communication.
It is derived from I²C for communication with low-bandwidth devices, especially power related chips. Other devices might include temperature or voltage sensors and clock chips. PCIEx add-in cards may connect to a SMBus segment.

The processor provides a SMBus 1.0-compliant host controller. The host controller provides a mechanism for the CPU to initiate communications with SMB peripherals (slaves).

Devices connected to the E660T SMBus:

IC	Function
U901 (TMP101)	DDR2 Ambient Temperature Sensor
U900 (LM95245)	Atom internal Temp. Sensor processing
U1300A (Intel 82574 Eth.- PHY)	The interface can be used to configure the 82574's filters and management related capabilities.
U102C (SDC)	System Diagnostic Controller (ADC, CAN, Reset Controlling)

Table 7: Devices connected by SMBus

4.8.1 Ambient Temperature Sensor

The ECUcore-E660 features a Temperature sensor TMP101 (U901) to record ambient temperatures to, e.g., enable protection from RAM overheating. The sensor is located directly between the DDR2-RAM ICs. The ECUcore-E660 just provides the physical connection

between the CPU and the sensor. The communication or any protective measures are software functions to be provided by the user application.

Temperature sensor characteristics:

- Temperature resolution of 0.0625°C
- Temperature range of -55°C to +125°C
- Alert pin as interrupt source if temperature exceeds defined limits

The Alert-Pin is connected to E660 to be used by the application (Pin AP19 (GPIO_B)).

4.8.2 E660 Internal Temperature Sensor

An internal temperature sensor of E660T can be used to determine overheating of CPU-Core. For this it is necessary to place an additional IC. The LM95245 precision remote diode digital temperature sensor has following characteristics:

- Temperature resolution of 0.0625°C
- Temperature range of -125°C to +125°C or from 0 to +255°C
- Alert pin as interrupt source if temperature exceeds defined limits

4.8.3 System Diagnostic Controller

The complexity of the high performing “Queens Bay” platform (Intel Atom E6xx + Intel EG20T Hub) makes it inevitable to add an own controller for guarding and managing purposes only. Therefore the ECUcore E660 houses a separate ARM controller (STM32F103) as so called System Diagnostic Controller (SDC).
The CPU and the SDC communicate through the SMBus interface with each other.

Following features provided by the SDC:

- Temperature and voltage guarding
- Reset handling

- Standby/Wakeup handling
- Additional CAN interface
- Analog-Digital-Conversion
- Additional GPIOs

4.9 SPI Module

The ECUcore-E660 allows high-speed serial communication with SPI devices such as EEPROM via two SPI interfaces, one directly from Atom E660T and one from EG20T Hub. The SPI interfaces contain two chip select (CS) signals each. The SPI bus signals are directly dumped via the board connector.

There is one EEPROM connected to the SPI on-board. The on-board EEPROM is connected to CSPI2 and occupy CSPI2_SS0.

The following table shows the available SPI signals.

	X1402-Pin	**Connector signal**	**SPI signal**	**Description**
Atom CPU	A26	/SPI_CS	/SPI_CS	SPI-Chip Select
	A25	SPI_MOSI	SPI_MTSR (SOUT)	Master Transmit Slave Receive
	A23	SPI_MISO	SPI_MRST (SIN)	Master Receive Slave Transmit
	A24	SPI_CLK	SPI_CLK (SCK)	Clock
EG20T Periphery Hub	**X1403-Pin**			
		/SPI2_CS	/SPI2_CS	SPI2-Chip Select
		SPI2_MOSI	SPI2_MTSR (SOUT)	Master Transmit Slave Receive
		SPI2_MISO	SPI2_MRST (SIN)	Master Receive Slave Transmit
		SPI2_CLK	SPI2_CLK (SCK)	Clock

Table 8: SPI Signals

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4.9.1 On-board EEPROM

The ECUcore-E660 is equipped with one on-board EEPROM. The EEPROM (default SST25VF016B 16MBit) is used to store bios configuration data. It is connected to the E660T via SPI module. The EEPROM uses the chip select /SPI_CS.

4.10 Display Support

To simplify the development of devices that require human machine interfaces, the ECUcore-E660 supports interfacing LCD and TFT displays directly. The Intel® Atom™ Processor E6xx Series supports LVDS and Serial DVO display ports permitting simultaneous independent operation of two displays.
The ECUcore-E660 always includes this LVDS and SDVO interface.

4.10.1 LVDS Interface

The E660 supports a Low-Voltage Differential Signaling interface that allows the Graphics and Video adaptor to communicate directly to an onboard flat-panel display. The LVDS interface supports pixel color depths of 18 and 24 bits, maximum resolution up to 1280x768 @ 60 Hz. Minimum pixel clock is 19.75 MHz. Maximum pixel clock rate up to 80 MHz.
The processor does provide LVDS backlight control related signals in order to support LVDS panel backlight adjustment.
The ECUcore-E660 is designed to use a maximum pixel depth of 24bits. The following table shows the signals that are dumped out of the board via X1402

X1402-Pin	Connector signal	LVDS signal
A13	LCD_DATA0+	TXOUT0+
A14	LCD_DATA0-	TXOUT0-
A15	LCD_DATA1+	TXOUT1+
A16	LCD_DATA1-	TXOUT1-
A17	LCD_DATA2+	TXOUT2+
A18	LCD_DATA2-	TXOUT2-
A19	LCD_DATA3+	TXOUT3+
A20	LCD_DATA3-	TXOUT3-
A21	LCD_CLK+	TxCLK OUT+
A22	LCD_CLK-	TxCLK OUT-

Table 9: LVDS controller signals

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4.10.2 SDVO Interface

Digital display channel capable of driving SDVO adapters that provide interfaces to a variety of external display technologies (e.g., DVI, TV-Out, analog CRT).

- Maximum resolution up to 1280x1024 @ 85 Hz.
- Maximum pixel clock rate up to 160 MHz.

SDVO lane reversal is not supported.

The following table shows the signals that are dumped out of the board via X1402

X1402-Pin	Connector signal	Description
B13 B14	SDVO_RED+ SDVO_RED-	Differential Serial Digital Video Red
B15 B16	SDVO_GREEN+ SDVO_GREEN-	Differential Serial Digital Video Green
B17 B18	SDVO_BLUE+ SDVO_BLUE-	Differential Serial Digital Video Blue
B19 B20	SDVO_INT+ SDVO_INT-	Differential interrupt input
B21 B22	SDVO_CLK+ SDVO_CLK-	Differential clock signal (runs between 100 MHz and 200 MHz)
B23 B24	SDVO_TVCLKIN+ SDVO_TVCLKIN-	Differential TV-OUT Synchronization Clock
B25 B26	SDVO_STALL+ SDVO_STALL-	Differential input. Allows a scaling SDVO device to stall the pixel pipeline
B27	SDVO_CTRLCLK	Single-ended control clock line to the SDVO device.
B28	SDVO_CTRLDATA	Is used in conjunction with SDVO_CTRLCLK to transfer device config, PROM, and monitor DDC information

Table 10: SVDO signals

4.11 CAN Interface

The ECUcore-E660 includes two CAN interfaces. One is placed directly by the EG20T Periphery Hub (PCH) and one by the SDC. In cause of disaffected behavior at the EG20T CAN interface it is recommended to use the CAN-Interface provided by SDC.

Both interfaces are dumped out to X1401 connector:

X1401-Pin	**Signal**
B3	CAN_RX (PCH)
B4	CAN_TX (PCH)
A39	SDC_CANRX (SDC)
A40	SDC_CANTX (SDC)

Table 11: CAN Signals

4.12 Serial Interface

The ECUcore-E660 supports up to 4 independent UARTs. They feature individual baud rate generators.

UART0 ie available on the board connector with the following lines: RXD, TXD, CTS, RTS and SCK.

UART1-3 only features 2-wire UARTs.

Features:

- Supports full UART and 2-wire UART
  - UART0: full UART
  - UART1-3: 2-wire UART
- Full-duplex buffering
- Full status reporting

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- Reduces interrupts to CPU by implementing 256-bytes(UART0) or 64-bytes(UART1-3) transmit and receive FIFOs
- Independent control of the following: transmission interrupt, reception interrupt, line status interrupt, and FIFOs
- Programmable serial interface
  - 5-, 6-, 7-, or 8-bit character
  - Generation and verification of odd parity, even parity, or no parity
  - 1, 1.5, and 2 stop bits
- •Programmable baud rate generator
  - UART0: from 300 bps to 4Mbps
  - UART1-3: from 300 bps to 1Mbps
- Equipped with DMA interface

Following UART-Signals dumped out to X1402:

X1402-Pin	**Signal**
A27	UART0_TX
A28	UART0_RX
B29	UART0_CTS
B30	UART0_DCD
B31	UART0_DSR
B32	UART0_DTR
B33	UART0_RI
B34	UART0_RTS
A30	UART1_TX
A31	UART1_RX
A32	UART2_TX
A33	UART2_RX
A34	UART3_TX
A35	UART3_RX

Table 12: UART Signals

4.13 SDCard/MMC Interface

The ECUcore-E660 supports two multimedia-card interfaces. Both MMC interfaces (SDIO0 and SDIO1) are brought out via connector. Each interface has 8 data pins for the usage as SD-Card or MMC interface.

Card Detect and Card Protect are supported by default on ECUcore-E660 pin connector.

4.14 USB Interfaces

The ECUcore-E660 provides six USB2.0 (480Mbit/s) host and one USB2.0 (480Mbit/s) device interfaces. Each interface is brought out at the connector.
No security components (such as TVS-Diodes) are provided at the module, they have to be mounted near the USB connector on the customer board.
Over-current protection is not supported by default. If necessary, use an external current limiting device with over-current-flag and connect it to one of the E660 USB-OVC pin.
Following USB-Signals dumped out to X1400:

X1402-Pin	Signal	Description
A22	USB_H4_POW_EN	USB Host 4 Port Power Enable
A23	/USB_H4_OVC	USB Host 4 Port Overcurrent Indication
A24	USB_H4_-	USB Host 4 Differential Data Bus
A25	USB_H4_+	
A26	USB0H2_POW_EN	USB Host 2 Port Power Enable
A27	/USB_H2_OVC	USB Host 2 Port Overcurrent Indication
A28	USB_H2_-	USB Host 2 Differential Data Bus
A29	USB_H2_+	
A30	USB_H0_POW_EN	USB Host 0 Port Power Enable
A31	/USB_H0_OVC	USB Host 0 Port Overcurrent Indication
A32	USB_H0_-	USB Host 0 Differential Data Bus

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Ord. No. L-1562e_01
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A33	USB_H0_+	
A34	USB_D_-	USB Device Differential Data Bus -
A35	USB_D_+	
B22	USB_H5_POW_EN	USB Host 5 Port Power Enable
B23	/USB_H5_OVC	USB Host 5 Port Overcurrent Indication
B24	USB_H5_-	USB Host 5 Differential Data Bus
B25	USB_H5_+	
B26	USB_H3_POW_EN	USB Host 3 Port Power Enable
B27	/USB_H3_OVC	USB Host 3 Port Overcurrent Indication
B28	USB_H3_-	USB Host 3 Differential Data Bus
B29	USB_H3_+	
B30	USB_H1_POW_EN	USB Host 1 Port Power Enable
B31	/USB_H1_OVC	USB Host 1 Port Overcurrent Indication
B32	USB_H1_-	USB Host 1 Differential Data Bus
B33	USB_H1_+	

Table 13: UART Signals

4.15 Serial HD Audio Interface

The Intel® High Definition Audio controller consists of a set of DMA engines that are used to move samples of digitally encoded data between system memory and an external codec(s). The controller communicates with the external codec(s) over the Intel® HD Audio serial link. The E660 implements two output DMA engines and two input DMA engines. The Output DMA engines move digital data from system memory to a D-A converter in a codec. The processor implements a single Serial Data Output signal (HDA_SDO) that is connected to all external codecs.
The Input DMA engines move digital data from the A-D converter in the codec to system memory. The processor supports up to two external codecs by implementing two Serial Data Input signals (HDA_SDI[1:0]), one dedicated to each of the supported codecs.
The external codec has to be placed on the customer board.

X1400-Pin	Signal	Description
A18	HDA_SYNC	This signal is an 48-kHz fixed rate sample sync to the codec(s).
A19	/HDA_RST	Reset for external Codec
A20	HDA_CLK	24MHz serial data clock with integrated pulldown
A21	HDA_SDO	serial TDM data output to the codec(s)
B18 B19	HDA_SDI1 HDA_SDI0	serial TDM data input to the codec(s) with integrated pulldown
B20	/HAD_DOCKEN	This active low signal controls the external Intel® HD Audio docking isolation logic
B21	/HAD_DOCKRST	This signal is a dedicated reset signal for the codec(s) in the docking station. It works similar to, but independent of, the normal HDA_RST_B signal.

Table 14: HD Audio signals

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4.16 LPC Interface

The LPC controller implements a low pin count interface that supports the LPC 1.1 specification:

- LSMI_B can be connected to any of the SMI capable GPIO signals.
- The EC's PME_B should connect it to GPE_B.
- The LPC controller's SUS_STAT_B signal is connected directly to the LPCPD_B signal.

The LPC controller does not implement DMA or bus mastering cycles.

The LPC Bus at ECUcore E660 is directly dumped out to X1400 Pin B1 to B9.

5 Technical Data

The physical dimension of the ECUcore-E660 is shown in the figure below.

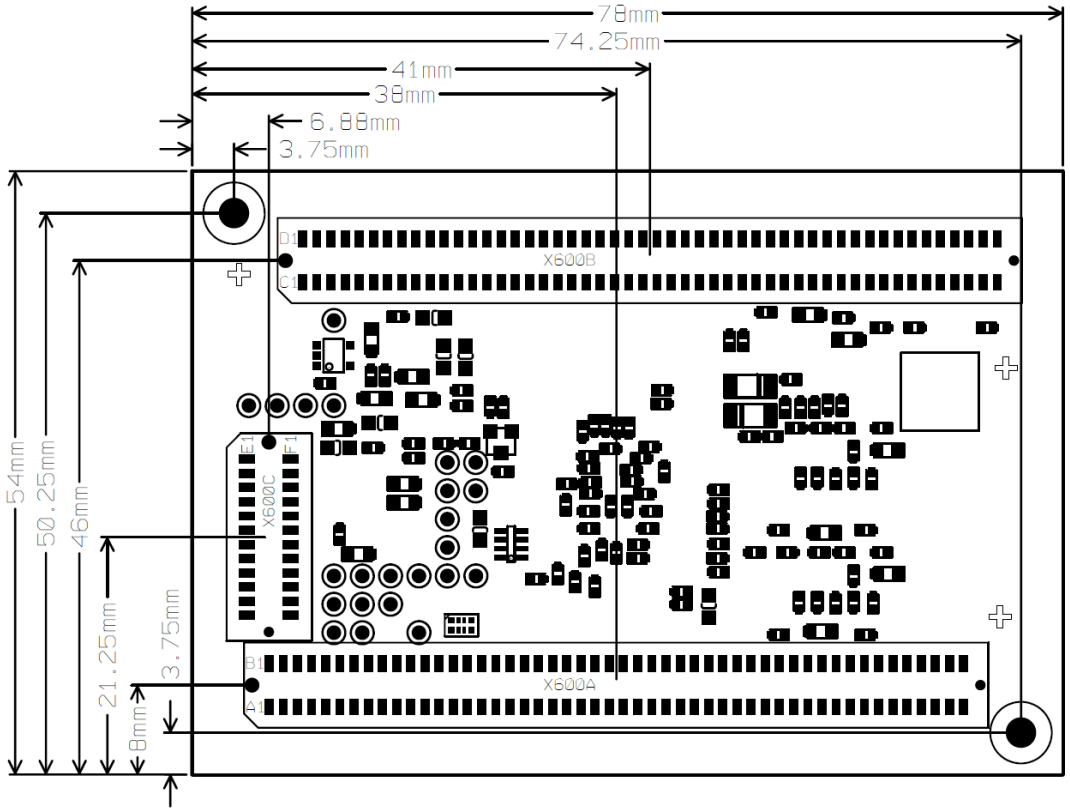

Figure 4: Physical Dimensions

The height including the board connector and components is about 8mm. The thickness of the PCB is about 1.6mm. The maximum component height on top is about 3mm.

dimensions	78mm x 54mm x 8mm
weight	approximately 21,5g
operating temperature	-40°C to +85°C
storage temperature	-40°C to +85°C
operating voltage	3.3V DC ± 5%
current consumption	typ. 820mA
I/O-Level	3.3V DC ± 5%

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Table 15: Technical Data

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Document number:	L-1562e_01, Edition July 2014

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